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Attachment I

(Pictures of the EUT and Electrical Schemes)



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1.1 PICTURES



Front 1



Front 2





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Front 1



Front 2





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Left Side



Rigt Side

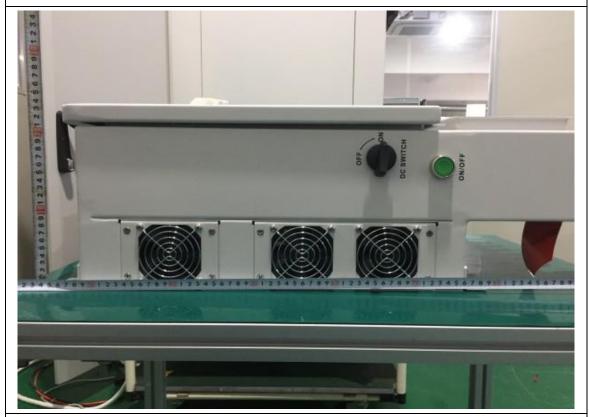




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IP65

Left Side



Rigt Side

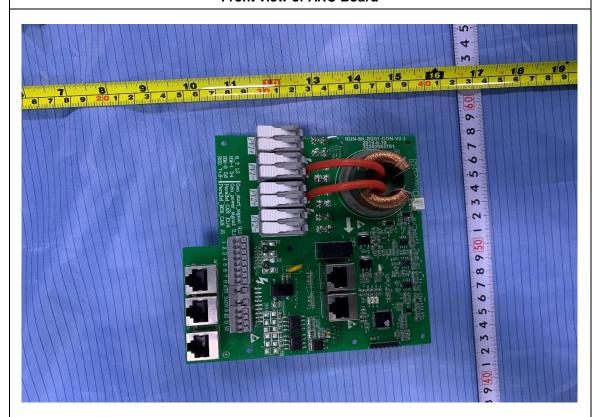




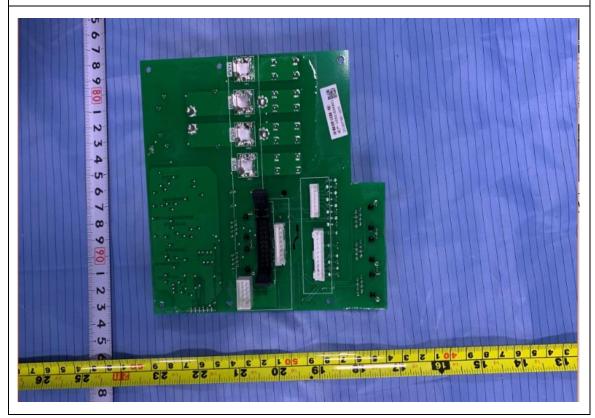
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IP20

Front view of ARC Board



Back view of ARC Board





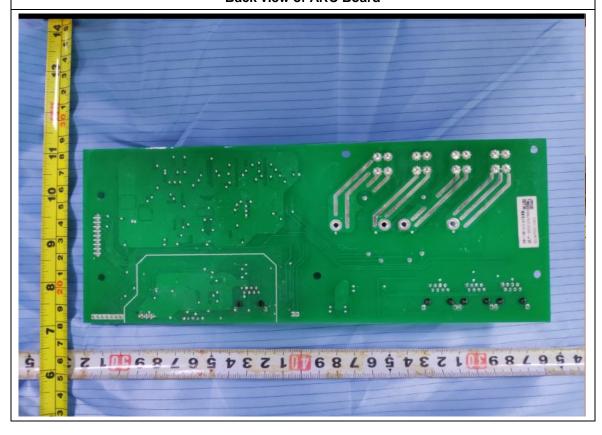
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IP65

Front view of ARC Board



Back view of ARC Board

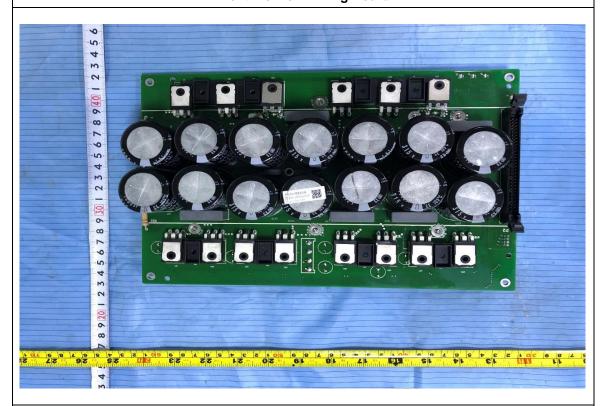




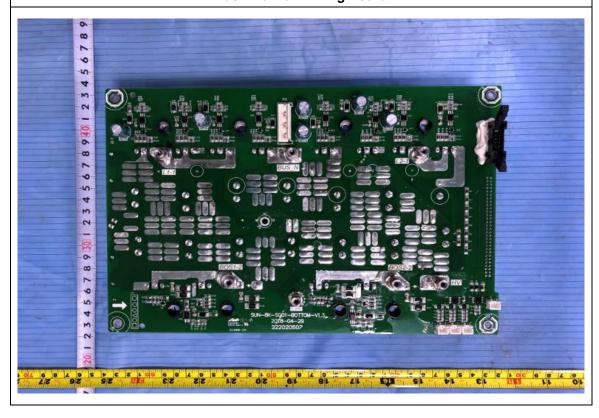
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IP20

Front view of Driving Board



Back view of Driving Board





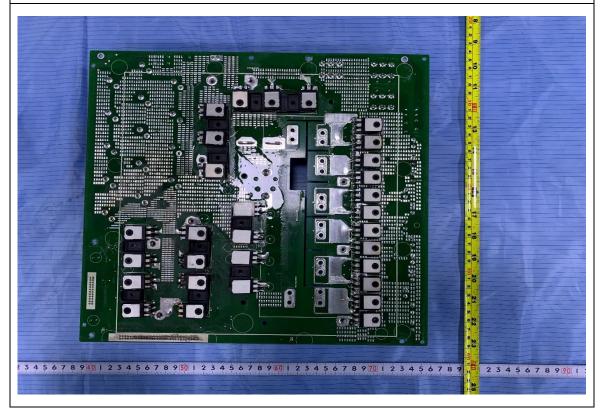
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Front view of Driving Board



Back view of Driving Board

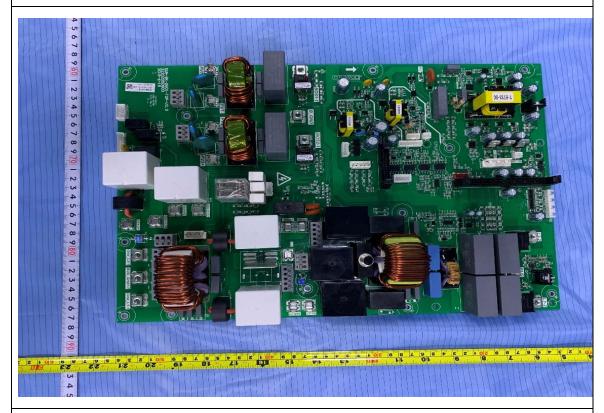




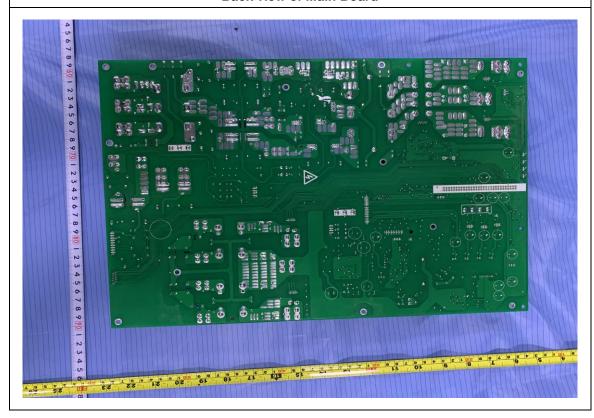
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IP20

Front view of Main Board



Back view of Main Board

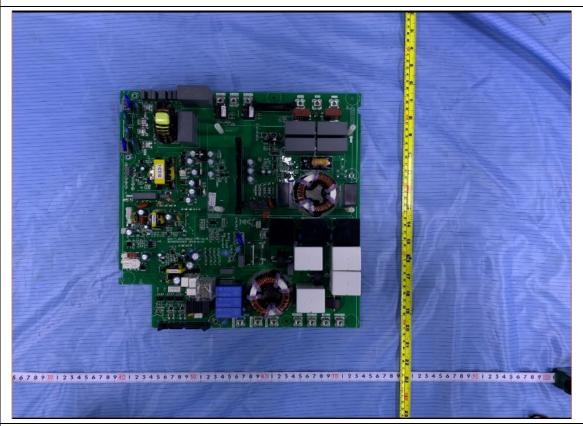




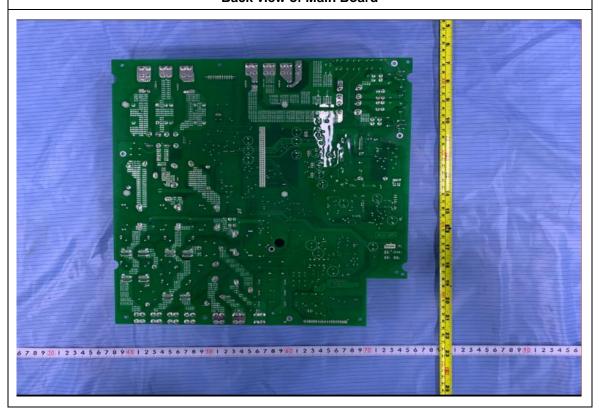
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Front view of Main Board



Back view of Main Board





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Front view of Control Board



Back view of Control Board





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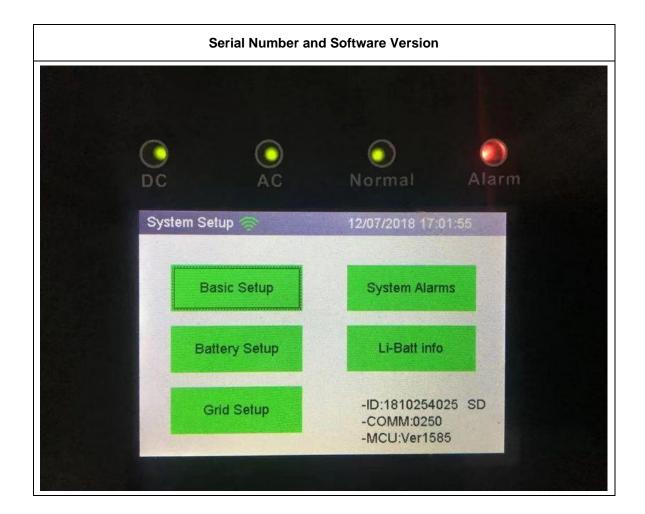
Back view of Display Board







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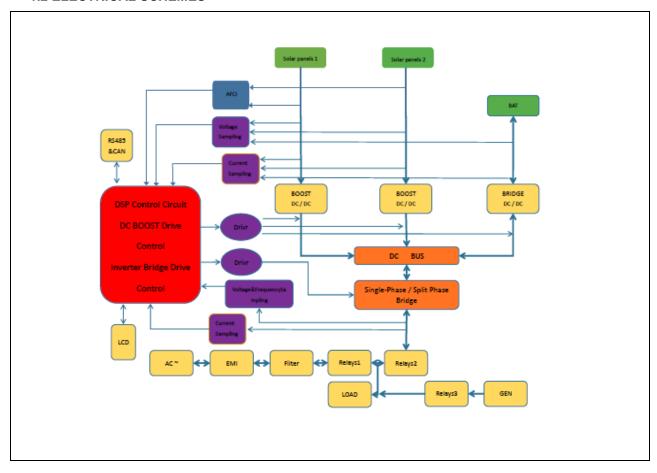
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1.2 ELECTRICAL SCHEMES





Attachment II

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Attachment II

(Testing information)



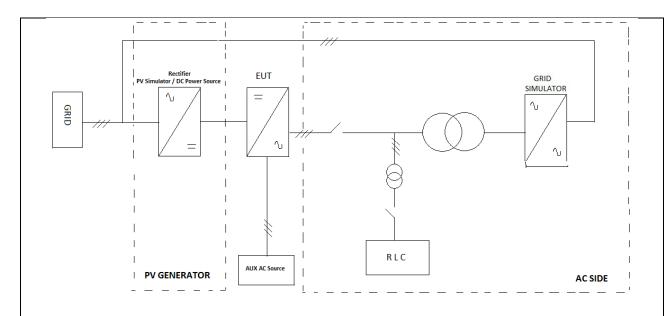
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2.1 TESTING CIRCUIT



Different equipment has been used to take measures as it shows in testing equipment list.

Current and voltage clamps have been connected to the inverter output for all the tests.

All the tests described in the following pages have used this specified test setup.

2.2 MEASUREMENT UNCERTAINTY

Magnitude	Uncertainty
Voltage measurement uncertainty	±1.5 %
Current measurement uncertainty	±2.0 %
Frequency measurement uncertainty	±0.2 %
Time measurement uncertainty	±0.2 %
Power measurement uncertainty	±2.5 %
Phase Angle	±10
Temperature	±3° C

Note1: Measurements uncertainties showed in this table are maximum allowable uncertainties. The measurement uncertainties associated with other parameters measured during the tests are in the laboratory at disposal of the solicitant.